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DISPLAY DEVICE BUSSINESS GROUP
SHARP CORPORATION

SPECIFICATION

DEVICE SPECIFICATION FOR

TFT-LCD Open Cell

Model No. LK315D3HA9K

CUSTOMER'S APPROVAL

DATE

PRESENTED

BY

BY K. Tanaka
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SHARP CORPORATION

RECORDS OF REVISION

MODEL No. : LK315D3HA9K

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-K23510	Apr. 12, 2013	-	-	-	1st ISSUE
	Apr. 22, 2013	A	P16	- Revision of the ESD test condition. ▲A	2nd ISSUE
	Jun.19,2013	B	P2	- Change the surface resistance of the protection film defined side. ▲B-1	3rd ISSUE
			P8	- Change of t5 minimum definition. ▲B-2	
			P15	- Change of the content indicated in Model No. Area of the Cell Box Label and the Palette Label. ▲B-3	
			P20	- Correction of the surface resistance of the Cell Box. ▲B-4	

1. Application

This specification applies to the color 31.5 inch TFT-LCD Open Cell LK315D3HA9K.

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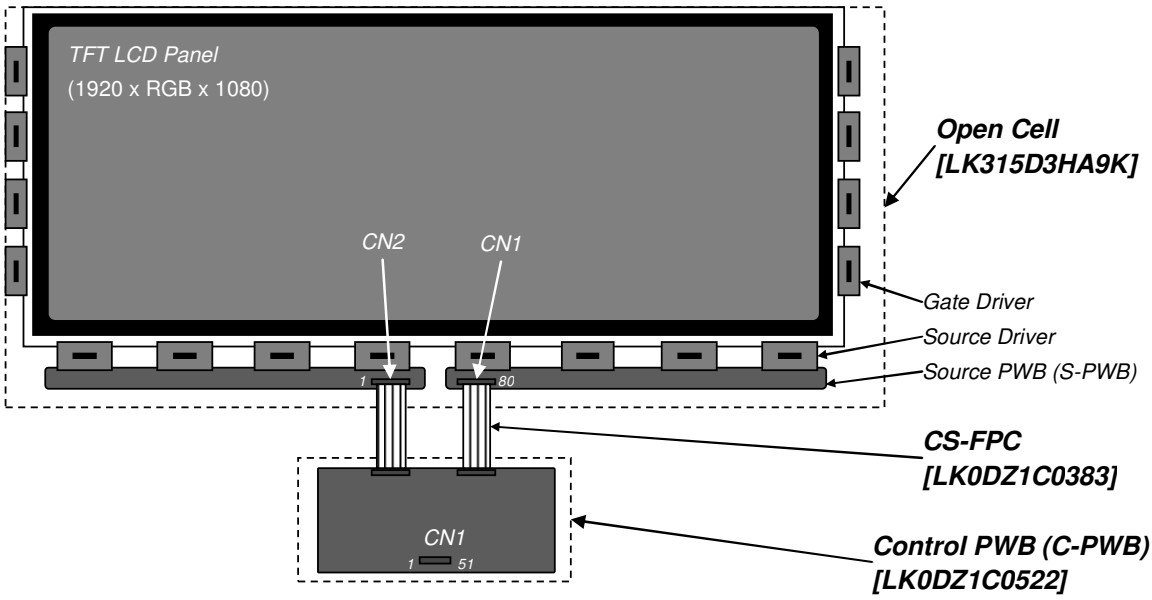
2. Overview

This Open Cell is a color-active-matrix-LCD-Open-Cell incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, Source PWBs.

The following contents can be achieved in using LK0DZ1C0522 (Timing Control-PWB) and LK0DZ1C0383 (Control-Source-FPC) that SHARP specifies.

Graphics and texts can be displayed on a 1920 x RGB x 1080 dots panel with about seventeen million colors by using 8bit LVDS (Low Voltage Differential Signaling) to interface, +12V of DC supply voltages.

And in order to display the moving picture smoothly, this Open Cell and C-PWB supports the Over Shoot driving (OS driving) technology on the Single Frame Rate (SFR). In the OS driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.



3. Mechanical Specifications

Parameters	Specifications	Unit
Display size	80.131 (Diagonal)	cm
	31.5475 (Diagonal)	inch
Active area	698.40 (H) x 382.85 (V)	mm
Pixel format	1920 (H) x 1080 (V) (1pixel = R + G + B dot)	pixel
Pixel pitch	0.36375 (H) x 0.36375 (V)	mm
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally black	
Outline dimensions [Note1]	723.08 (H) x 444.4 (V) x 2.85 (D)	mm
Mass	1.3±0.3	kg
Surface treatment [Note2,3]	- Front polarizer : Super Low Haze Anti Glare Hard coating 2H and more, Haze: Less than 3% - Rear polarizer : Hard coating less (B)	

[Note1] The thickest point is 80pin CN of S-PWB, the polarizer area thickness is shown the outline drawing in P19.

[Note2] With the protection film removed.

[Note3] Surface resistance of the protection film adhesive side is 10^{10} ohm/sq. ▲B-1

4. Open Cell Driving Specifications

4.1. Driving Interface of C-PWB SHARP specifies [LK0DZ1C0522]

CN1: Power and LVDS data input

- Using connector: FI-RNE51SZ-HF (Japan Aviation Electronics Ind., Ltd.)
- Mating connector: FI-RE51HL, FI-RE51CL or equivalent device (Japan Aviation Electronics Ind., Ltd.)
- Mating LVDS transmitter: THC63LVD1023 or equivalent device

Pin No.	Symbol	Function	Remark
1	P_VCC	+12V Power Supply	
2	P_VCC	+12V Power Supply	
3	P_VCC	+12V Power Supply	
4	P_VCC	+12V Power Supply	
5	P_VCC	+12V Power Supply	
6	NC	It is required to set non-connection (OPEN)	
7	GND		
8	GND		
9	GND		
10	CH1_0-	LVDS differential data input	
11	CH1_0+	LVDS differential data input	
12	CH1_1-	LVDS differential data input	
13	CH1_1+	LVDS differential data input	
14	CH1_2-	LVDS differential data input	
15	CH1_2+	LVDS differential data input	
16	GND		
17	CH1_CLK-	LVDS Clock signal	
18	CH1_CLK+	LVDS Clock signal	
19	GND		
20	CH1_3-	LVDS differential data input	
21	CH1_3+	LVDS differential data input	
22	Reserved		
23	Reserved		
24	GND		
25	CH3_0-	LVDS differential data input	
26	CH3_0+	LVDS differential data input	

27	CH3_1-	LVDS differential data input	
28	CH3_1+	LVDS differential data input	
29	CH3_2-	LVDS differential data input	
30	CH3_2+	LVDS differential data input	
31	GND		
32	CH3_CLK-	LVDS Clock signal	
33	CH3_CLK+	LVDS Clock signal	
34	GND		
35	CH3_3-	LVDS differential data input	
36	CH3_3+	LVDS differential data input	
37	Reserved		
38	Reserved		
39	GND		
40	SCL_I	I2C CLK	Pull up: 3.3V [Note1]
41	NC	It is required to set non-connection (OPEN)	
42	NC	It is required to set non-connection (OPEN)	
43	WP	I2C bus enable (L/Open: disable, H: enable)	[Note2]
44	SDA_I	I2C DATA	Pull up: 3.3V [Note1]
45	LVDS_SEL	Select LVDS data order [Note4]	Pull down: GND [Note3]
46	BIST_EN	Test pattern enable (L/Open: enable, H: disable)	[Note4]
47	NC	It is required to set non-connection (OPEN)	
48	NC	It is required to set non-connection (OPEN)	
49	NC	It is required to set non-connection (OPEN)	
50	NC	It is required to set non-connection (OPEN)	
51	NC	It is required to set non-connection (OPEN)	

CN3: Aging Test Pattern Control

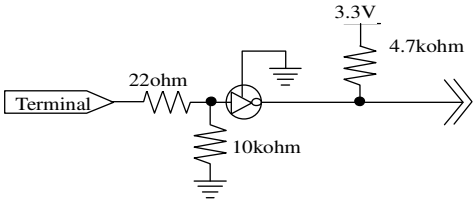
- Using connector: 20037WR-08 (YeonHo)

Pin No.	Symbol	Function	Remark
1	VDD12V	+12V Power Supply	
2	VDD12V	+12V Power Supply	
3	GND		
4	A_EN	Test pattern enable (L/Open: enable, H: disable)	[Note4]
5	WP	I2C bus enable (L/Open: disable, H: enable)	[Note2]
6	SDA	I2C DATA	Pull up: 3.3V [Note1]
7	SCL	I2C CLK	Pull up: 3.3V [Note1]
8	GND		

[Note] GND of a liquid crystal panel drive part should be connected with a module chassis.

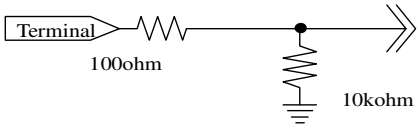
[Note1] The equivalent circuit figure of the terminal for SCL_I, SDA_I.

[Note2] The equivalent circuit figure of the terminal for WP.

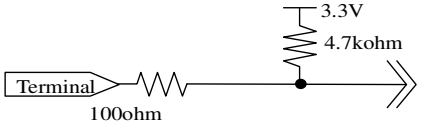


I2C control is for EDID writing and Vcom adjustment.

[Note3] The equivalent circuit figure of the terminal for LVDS_SEL.



[Note4] The equivalent circuit figure of the terminal for BIST_EN, A_EN.

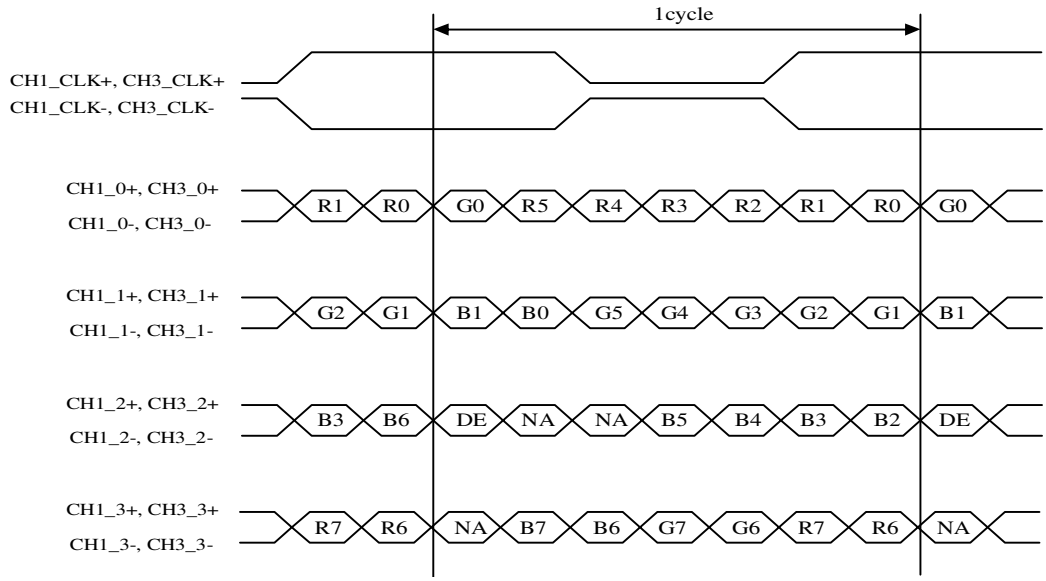


[Note5] LVDS Data order

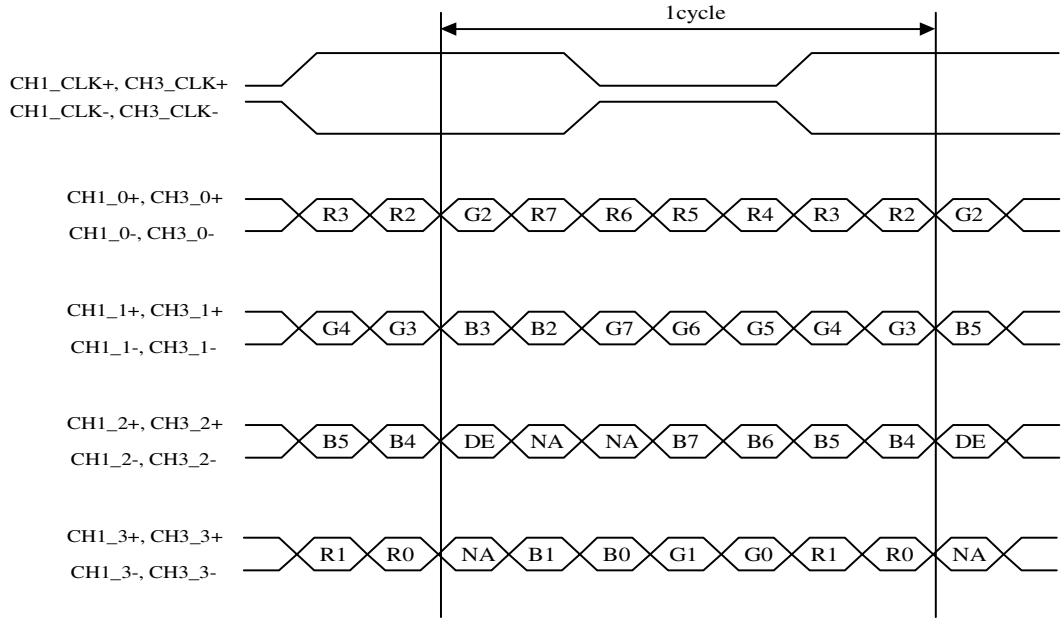
LVDS_SEL		
Data	H(3.3V) [VESA]	L(GND) or Open [JEIDA]
TA0	R0(LSB)	R2
TA1	R1	R3
TA2	R2	R4
TA3	R3	R5
TA4	R4	R6
TA5	R5	R7(MSB)
TA6	G0(LSB)	G2
TB0	G1	G3
TB1	G2	G4
TB2	G3	G5
TB3	G4	G6
TB4	G5	G7(MSB)
TB5	B0(LSB)	B2
TB6	B1	B3
TC0	B2	B4
TC1	B3	B5
TC2	B4	B6
TC3	B5	B7(MSB)
TC4	NA	NA
TC5	NA	NA
TC6	DE(*)	DE(*)
TD0	R6	R0
TD1	R7	R1
TD2	G6	G0
TD3	G7	G1
TD4	B6	B0
TD5	B7	B1
TD6	N/A	N/A

NA: Not Available
(*)Since the display position is prescribed by the rise of DE (Display Enable) signal, please do not fix DE signal during operation at ”High”.

LVDS_SEL = High (3.3V) : VESA



LVDS_SEL = Low (GND) or OPEN : JEIDA

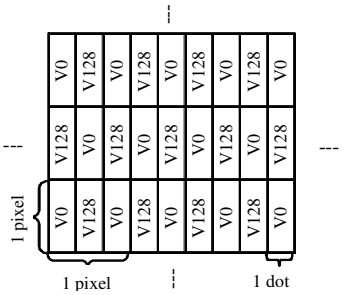


DE: Display Enable, NA: Not Available (Fixed Low)

4.2. Vcom adjustment

For the prevention of long-time image sticking of TFT-LCD panel, be sure to adjust Vcom in such ways that flicker is minimum on the center of display by visual or flicker meter.

- Vcom IC : MAX9684ETP+ (Maxim Integrated Products, Inc.) for I2C control from CN1 (Pin No. 40, 43, 44) or CN3 (Pin No.5,6,7) of C-PWB SHARP specifies [LK0DZ1C0522]
- Adjustment pattern :



4.3. Driving interface of S-PWB

CN1 and CN2 on the S-PWB: Input signal from C-PWB

- Using connector: 04 6806 080 000 846+ (KYOCERA Connector Products) or equivalent connector

Pin No.	CN1	CN2
1	GND	GND
2	Gate Power (L)	Gate Power (L)
3	Gate Power (H)	Gate Power (H)
4	Gate Start Pulse2	Gate Start Pulse 2
5	Gate Start Pulse1	Gate Start Pulse 1
6	Gate Clock	Gate Clock
7	Gate Output Enable	Gate Output Enable
8	Gate Scan Control	Gate Scan Control
9	MPD Control 1	MPD Control 1
10	MPD Control 2	MPD Control 2
11	MPD Control 3	MPD Control 3
12	MPD Control 4	MPD Control 4
13	MPD Control 5	MPD Control 5
14	MPD Control 6	MPD Control 6
15	MPD Control 7	MPD Control 7
16	MPD Control 8	MPD Control 8
17	MPD Control 9	MPD Control 9
18	MPD Control 10	MPD Control 10
19	MPD Control 11	MPD Control 11
20	MPD Control 12	MPD Control 12
21	Vcom	Vcom
22	Gray Level 9 (H)	Gray Level 9 (H)
23	Gray Level 8 (H)	Gray Level 8 (H)
24	Gray Level 7 (H)	Gray Level 7 (H)
25	Gray Level 6 (H)	Gray Level 6 (H)
26	Gray Level 5 (H)	Gray Level 5 (H)
27	Gray Level 4 (H)	Gray Level 4 (H)
28	Gray Level 3 (H)	Gray Level 3 (H)
29	Gray Level 2 (H)	Gray Level 2 (H)
30	Gray Level 1 (H)	Gray Level 1 (H)
31	miniLVDS data(+)	GND
32	miniLVDS data(-)	GND
33	miniLVDS data(+)	GND
34	miniLVDS data(-)	GND
35	miniLVDS data(+)	GND
36	miniLVDS data(-)	GND
37	GND	GND
38	miniLVDS clock(+)	GND
39	miniLVDS clock(-)	GND
40	GND	GND
41	miniLVDS data(+)	GND
42	miniLVDS data(-)	GND
43	miniLVDS data(+)	GND
44	miniLVDS data(-)	miniLVDS Cascade Control 2
45	miniLVDS data(+)	miniLVDS Scan Control
46	miniLVDS data(-)	miniLVDS Cascade Control 1
47	Logic Circuit Power	Logic Circuit Power
48	Logic Circuit Power	Logic Circuit Power
49	Reserved	Reserved
50	Polarity Control	Polarity Control

51	Latch Strobe	Latch Strobe
52	GND	GND
53	miniLVDS Cascade Control 2	miniLVDS data(+)
54	miniLVDS Scan Control	miniLVDS data(-)
55	miniLVDS Cascade Control 1	miniLVDS data(+)
56	GND	miniLVDS data(-)
57	GND	miniLVDS data(+)
58	GND	miniLVDS data(-)
59	GND	GND
60	GND	miniLVDS clock(+)
61	GND	miniLVDS clock(-)
62	GND	GND
63	GND	miniLVDS data(+)
64	GND	miniLVDS data(-)
65	GND	miniLVDS data(+)
66	GND	miniLVDS data(-)
67	GND	miniLVDS data(+)
68	GND	miniLVDS data(-)
69	Analog circuit power	Analog circuit power
70	Analog circuit power	Analog circuit power
71	Gray Level 1 (L)	Gray Level 1 (L)
72	Gray Level 2 (L)	Gray Level 2 (L)
73	Gray Level 3 (L)	Gray Level 3 (L)
74	Gray Level 4 (L)	Gray Level 4 (L)
75	Gray Level 5 (L)	Gray Level 5 (L)
76	Gray Level 6 (L)	Gray Level 6 (L)
77	Gray Level 7 (L)	Gray Level 7 (L)
78	Gray Level 8 (L)	Gray Level 8 (L)
79	Gray Level 9 (L)	Gray Level 9 (L)
80	GND	GND

4.4. Electrical characteristics of input voltage

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage	V_I	Ta=25°C	-0.3 ~ 3.6	V	[Note1]
12V supply voltage	VCC	Ta=25°C	0 ~ +14	V	
LVDS Voltage	VLVDS	Ta=25 °C	-0.3 ~ 3	V	[Note2]
Storage temperature	Tstg	-	-25 ~ +60	°C	[Note3]
Operation temperature	Topa	-	0 ~ +60	°C	[Note3]

[Note1] LVDS_SEL, I2C_SCL, I2C_SDA, WP

[Note2] CH1_CLK±, CH1_0±, CH1_1±, CH1_2±, CH1_3±,
CH3_CLK±, CH3_0±, CH3_1±, CH3_2±, CH3_3±

[Note3]

- Humidity: 95%RH Max.(Ta ≦ 40°C)
- Maximum wet-bulb temperature at 39°C or less. (Ta > 40°C)
- No condensation.
- Be sure to design the module with maintaining temperature of the panel at 60°C or less and uniform as much as possible. Otherwise there is possibility to cause several issue such as Mura or Gamma shift, etc.
- Be sure to follow the each part's recommended conditions of use about the part of producing heat itself, driver IC.

4.5. Electrical characteristics of input signals

Ta=25°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+12V supply voltage	Supply voltage	Vcc	11.4	12.0	12.6	V	[Note1]
	Current dissipation	Icc	-	0.8	2.9	A	[Note2]
	Inrush current	$I_{RUSH}1$	-	2.5	-	A	t1=500us [Note5]
		$I_{RUSH}2$	-	1.2	-	A	t1>5ms
Permissible input ripple voltage		V_{RP}	-	-	100	mV_{P-P}	Vcc = +12.0V
Input Low voltage		V_{IL}	0	-	0.7	V	[Note3]
Input High voltage		V_{IH}	2.3	-	3.3	V	
Input leak current (High)		I_{IH1}	-	-	400	μA	V_I = 3.3V [Note3]
Terminal resistor		R_T	-	100	-	ohm	Differential input
Input Differential voltage		|VID|	200	400	600	mV	[Note4]
Differential input common mode voltage		V_{CM}	|VID|/2	1.2	2.4-|VID|/2	V	[Note4]

[Note] V_{CM}: Common mode voltage of LVDS driver.

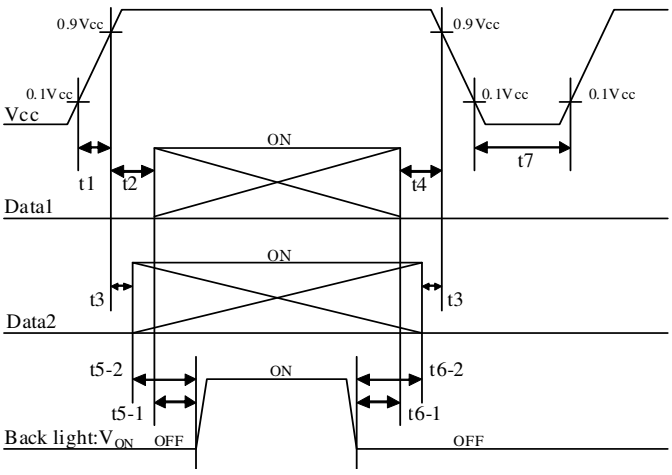
[Note1]

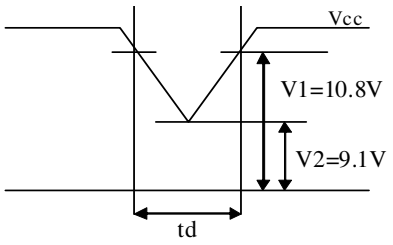
Input voltage sequences

50us < t1 < 20ms
20ms < t2 < 5s
20ms < t3 < 5s
0 < t4 < 1s
700ms < t5-1 ▲B-2
700ms < t5-2 ▲B-2
0 < t6 -1
0 < t6 -2
1s < t7

Dip conditions for supply voltage

a) V2 ≤ Vcc < V1
td < 10ms
b) Vcc < V2
This case is based on input voltage sequences.



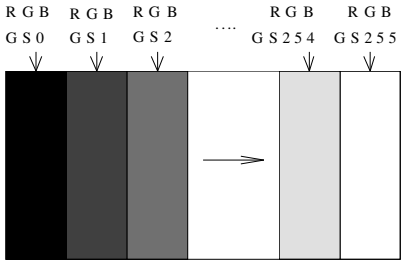


※ Data1: CH1_CLK±, CH1_0±, CH1_1±, CH1_2±, CH1_3±
CH3_CLK±, CH3_0±, CH3_1±, CH3_2±, CH3_3±
*V_{CM} voltage pursues the sequence mentioned above.

※ Data2: LVDS_SEL, SCL_I, SDA_I, WP

[Note] About the relation between data input and back light lighting, please base on the above-mentioned input sequence. When back light is switched on before panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

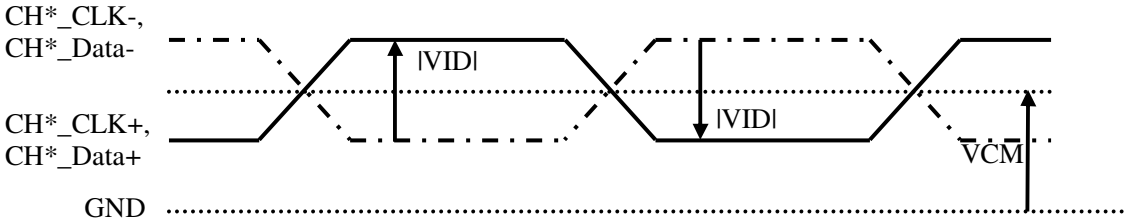
[Note2] Typical current situation: 255 gray-bar patterns. (Vcc = +12.0V)
The explanation of RGB gray scale is seen in section 4.8.



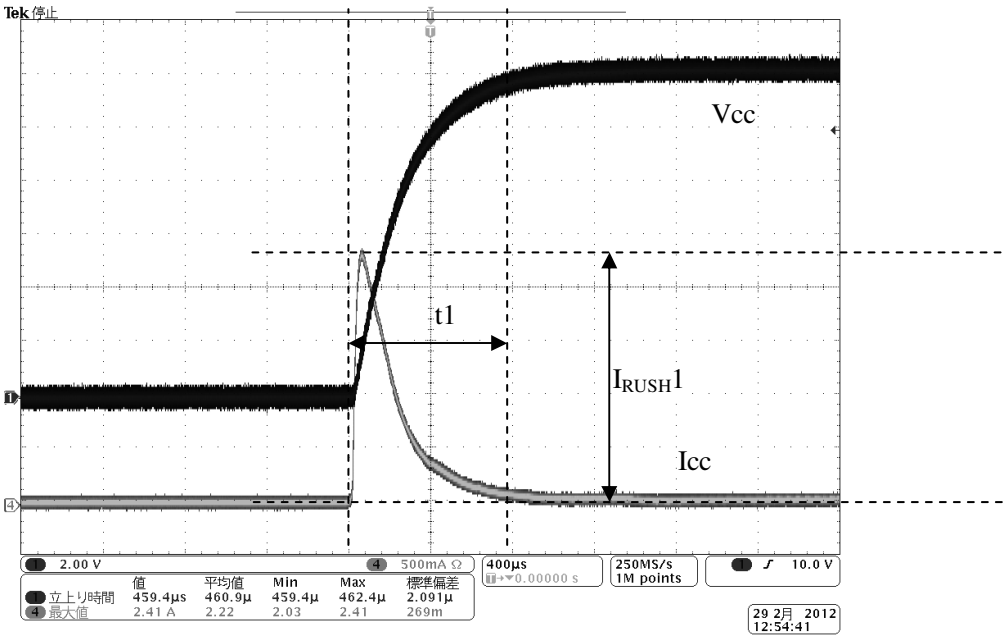
Vcc = +12.0V
1/Tc = 74.25MHz
TH = 14.8μs
TV = 60Hz

[Note3] LVDS_SEL, WP

[Note4] CH1_CLK±, CH1_0±, CH1_1±, CH1_2±, CH1_3±,
CH3_CLK±, CH3_0±, CH3_1±, CH3_2±, CH3_3±



[Note5] Vcc12V inrush current waveform



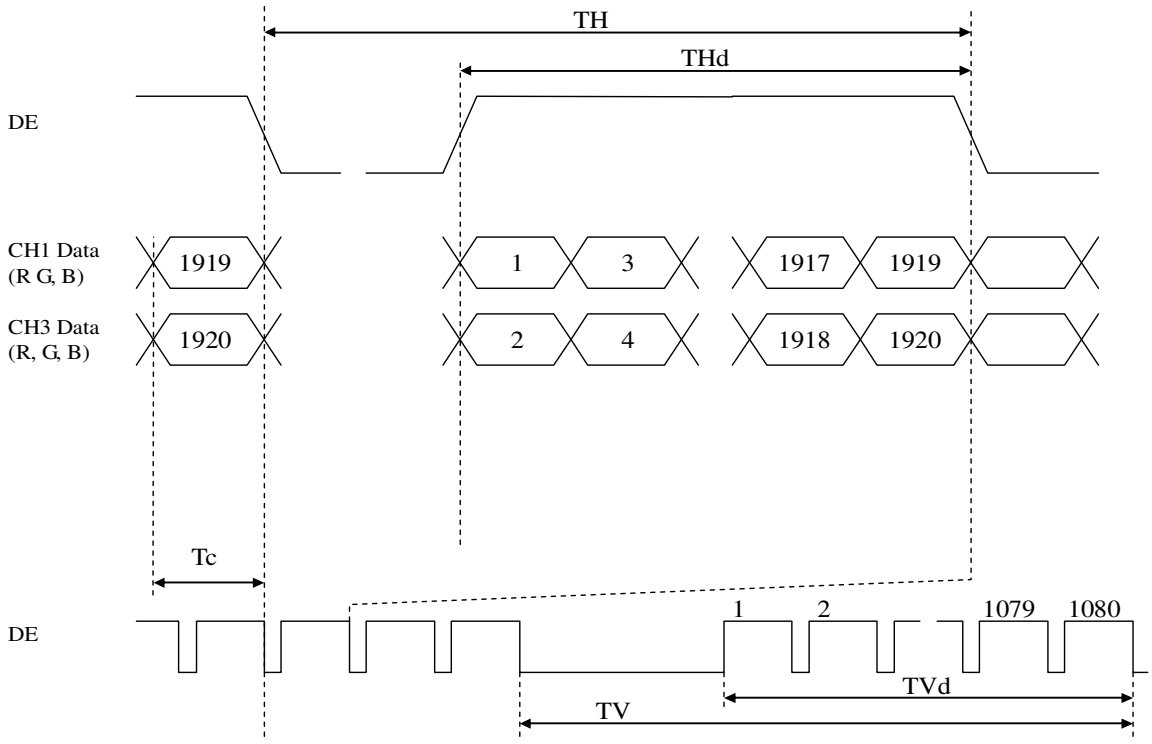
4.6. Timing characteristics of input signals

Timing diagrams of input signal are shown in below figure.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Clock	Frequency	1/Tc	69.0	74.25	76.0	MHz	
Data Enable Signal	Horizontal period	TH	1050	1100	1300	clock	
			14.2	14.8	16.1	µs	
	Horizontal period (High)	THd	960	960	960	clock	
	Vertical period	TV	1109	1125	1400	line	
			47	60	63	Hz	
	Vertical period (High)	TVd	1080	1080	1080	line	

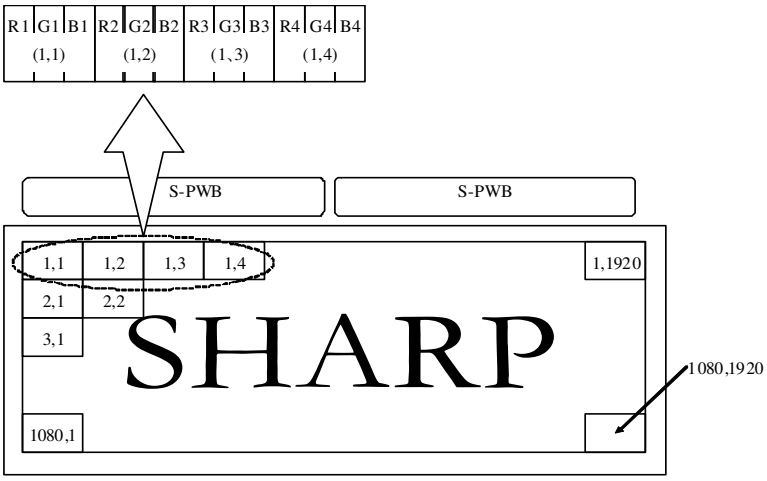
[Note]

- When vertical period is very long, flicker and etc. may occur.
- Please turn off the module after it shows the black screen.
- Please make sure that length of vertical period should become of an integral multiple of horizontal length of period. Otherwise, the screen may not display properly.
- As for your final setting of driving timing, we will conduct operation check test at our side, please inform your final setting.



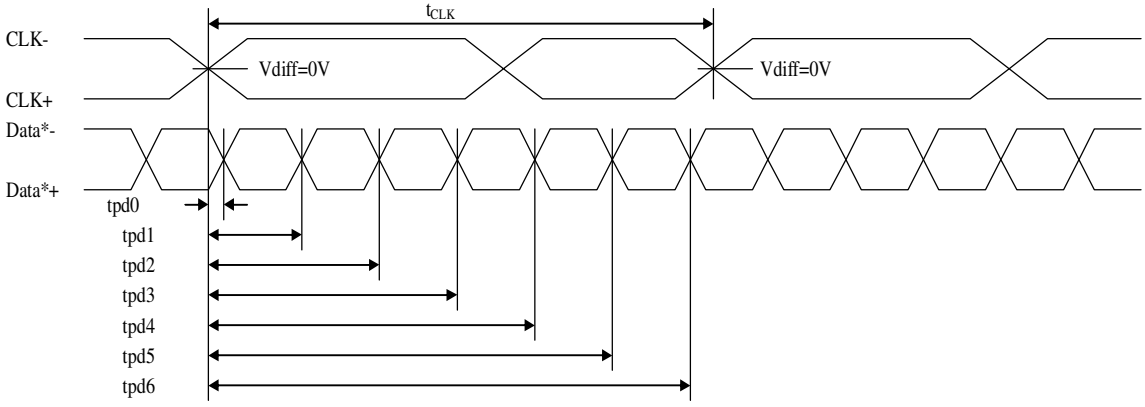
Timing diagram of input signal

4.7. Input data signal and display position on the screen



[Note] Scan direction is setting for using S-PWBs' side up. If you use S-PWB's side down, please invert the input of image.

4.8. Input data signal and display position on the screen



Item		Symbol	Min.	Typ.	Max.	Unit
Data position	Delay time, CLK rising edge to serial bit position 0	tpd0	-0.25	0	0.25	ns
	Delay time, CLK rising edge to serial bit position 1	tpd1	$1*t_{CLK}/7-0.25$	$1*t_{CLK}/7$	$1*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 2	tpd2	$2*t_{CLK}/7-0.25$	$2*t_{CLK}/7$	$2*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 3	tpd3	$3*t_{CLK}/7-0.25$	$3*t_{CLK}/7$	$3*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 4	tpd4	$4*t_{CLK}/7-0.25$	$4*t_{CLK}/7$	$4*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 5	tpd5	$5*t_{CLK}/7-0.25$	$5*t_{CLK}/7$	$5*t_{CLK}/7+0.25$	
	Delay time, CLK rising edge to serial bit position 6	tpd6	$6*t_{CLK}7-0.25$	$6*t_{CLK}/7$	$6*t_{CLK}/7+0.25$	

4.9. Input signal, basic display colors and gray scale of each color

Colors & Gray Scale			Data signal		
			R0R1R2R3R4R5R6R7 - -	G0G1G2G3G4G5G6G7 - -	B0B1B2B3B4B5B6B7 - -
Basic Color	Black	–	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	Blue	–	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	1 1 1 1 1 1 1 1 - -
	Green	–	0 0 0 0 0 0 0 0 - -	1 1 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -
	Cyan	–	0 0 0 0 0 0 0 0 - -	1 1 1 1 1 1 1 1 - -	1 1 1 1 1 1 1 1 - -
	Red	–	1 1 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	Magenta	–	1 1 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -	1 1 1 1 1 1 1 1 - -
	Yellow	–	1 1 1 1 1 1 1 1 - -	1 1 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -
	White	–	1 1 1 1 1 1 1 1 - -	1 1 1 1 1 1 1 1 - -	1 1 1 1 1 1 1 1 - -
Gray Scale of Red	Black	GS0	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	---	GS1	1 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	---	GS2	0 1 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	---	---	- -	- -	- -
	---	---	- -	- -	- -
	---	GS253	1 0 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	---	GS254	0 1 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	Red	GS255	1 1 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
Gray Scale of Green	Black	GS0	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	---	GS1	0 0 0 0 0 0 0 0 - -	1 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	---	GS2	0 0 0 0 0 0 0 0 - -	0 1 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	---	---	- -	- -	- -
	---	---	- -	- -	- -
	---	GS253	0 0 0 0 0 0 0 0 - -	1 0 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -
	---	GS254	0 0 0 0 0 0 0 0 - -	0 1 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -
	Green	GS255	0 0 0 0 0 0 0 0 - -	1 1 1 1 1 1 1 1 - -	0 0 0 0 0 0 0 0 - -
Gray Scale of Blue	Black	GS0	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -
	---	GS1	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	1 0 0 0 0 0 0 0 - -
	---	GS2	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	0 1 0 0 0 0 0 0 - -
	---	---	- -	- -	- -
	---	---	- -	- -	- -
	---	GS253	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	1 0 1 1 1 1 1 1 - -
	---	GS254	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	0 1 1 1 1 1 1 1 - -
	Blue	GS255	0 0 0 0 0 0 0 0 - -	0 0 0 0 0 0 0 0 - -	1 1 1 1 1 1 1 1 - -

- 0: Low level voltage / 1: High level voltage
- Each basic color can be displayed in 256 gray scales from 8 bits data signals. According to the combination of total 24 bits data signals, about 17 million-color display can be achieved on the screen.

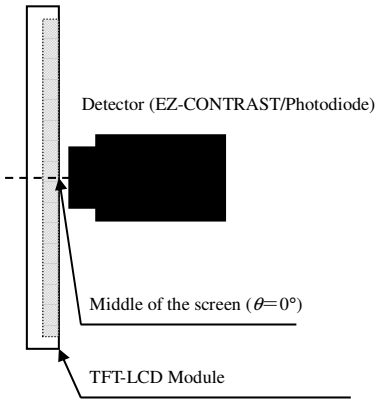
5. Optical Characteristics

Ta=25°C, Vcc=12.0V, Timing=60Hz (typ. value)

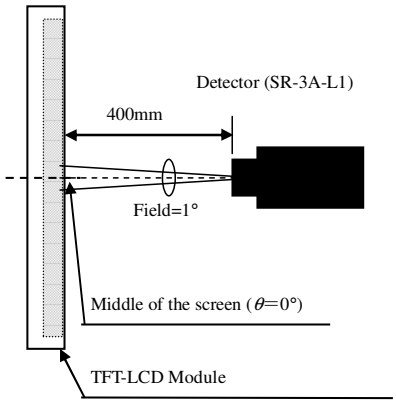
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ21 θ22	CR≧10	70	88	-	Deg.	[Note1,4]
	Vertical	θ11 θ12		70	88	-	Deg.	
Contrast ratio		CRn	θ=0 deg.	-	4000	-	-	[Note2,4]
Response time		τ_{DRV}		-	7	-	ms	[Note3,4,5]
Chromaticity	White	x		Typ-0.03	(0.280)	Typ+0.03	-	[Note4,7]
		y		Typ-0.03	(0.290)	Typ+0.03	-	
	Red	x		Typ-0.03	(0.645)	Typ+0.03	-	
		y		Typ-0.03	(0.330)	Typ+0.03	-	
	Green	x		Typ-0.03	(0.290)	Typ+0.03	-	
		y		Typ-0.03	(0.615)	Typ+0.03	-	
	Blue	x		Typ-0.03	(0.145)	Typ+0.03	-	
		y		Typ-0.03	(0.055)	Typ+0.03	-	
ACC		x		Typ-0.03	(Wx)	Typ+0.03	-	[Note4,7,8]
		y		Typ-0.03	(Wy)	Typ+0.03	-	
Luminance	White	Y_L		-	(350)	-	cd/m^2	[Note4,7]
Luminance uniformity	White	δw		-	-	(1.34)	-	[Note6]
Gamma		γ		Typ-0.35	(2.2)	Typ+0.35	-	[Note4,7,9]

- Optical characteristics (except Note7) are based on SHARP standard LED module's backlight system.
- Measurement condition: Set the maximum luminance of LED.
- The measurement shall be executed 60 minutes after lighting at rating.

[Note] The optical characteristics are measured using the following equipment.

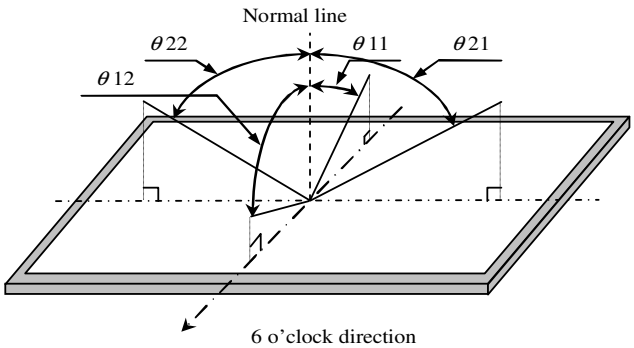


Measurement of viewing angle range and Response time.
-Viewing angle range: EZ-CONTRAST
- Response time: Photodiode



Measurement of Contrast, Luminance, Chromaticity.

[Note1] Definitions of the viewing angle range:



[Note2] Definition of the contrast ratio:
The contrast ratio is defined as the following.

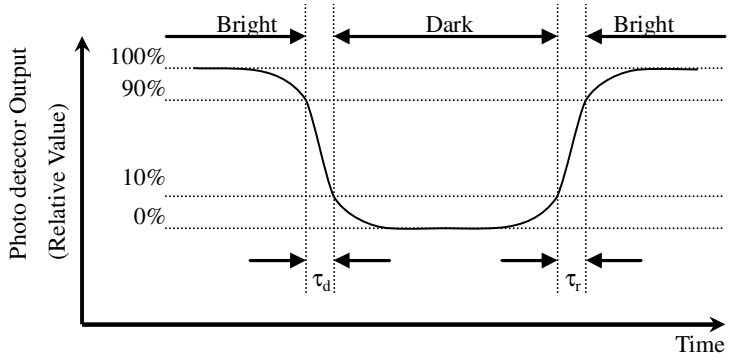
$$\text{Contrast Ratio} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

[Note3] Definition of the response time
The response time (τ_{rd}) is defined as the following.

$$\tau_{rd} = \{\sum(\text{tr} : x - y) + \sum(\text{td} : x - y)\}/20$$

τ_{rd} is the average value of the switching time from five gray levels (0%, 25%, 50%, 75% and 100%) to five gray levels (0%, 25%, 50%, 75% and 100%).

		Gray level of End (y)				
		0%	25%	50%	75%	100%
Gray level of Start (x)	0%		tr: 0%-25%	tr: 0%-50%	tr: 0%-75%	tr: 0%-100%
	25%	td: 25%-0%		tr: 25%-50%	tr: 25%-75%	tr: 25%-100%
	50%	td: 50%-0%	td: 50%-25%		tr: 50%-75%	tr: 50%-100%
	75%	td: 75%-0%	td: 75%-25%	td: 75%-50%		tr: 75%-100%
	100%	td: 100%-0%	td: 100%-25%	td: 100%-50%	td: 100%-75%	

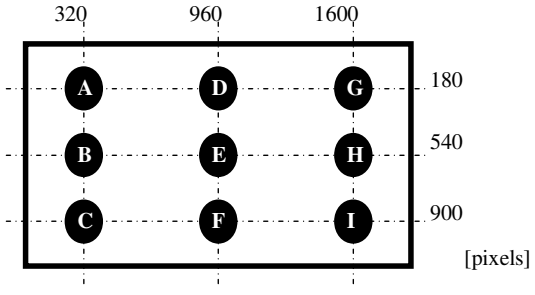


[Note 4] This value shall be measured at center of the active area.

[Note 5] This value is valid when O/S driving is used at typical input time value.

[Note 6] Definition of the white uniformity;
White uniformity is defined as the following with nine measurements. (A~I)

$$\delta w = \frac{\text{Maximum or Minimum luminance of nine points} - \text{Luminance of center point "E"}}{\text{Luminance of center points "E"}}$$



[Note7] These values are for reference based on measurement result by SEC backlight system and measurement conditions.
[Note8] Definition range of ACC is V32/255~V248/255.
[Note9] Definition range of Gamma is V50/255~V200/255.

6. Packing for Shipping

6.1. Packing Form

	1 palette	1 box
Size	1200 x 1000 x 1003(H) [mm]	831 x 558.5 x 129(H) [mm]
Q'ty	238 open cells	17 open cells
Mass	Max. 330 kg	Max. 22 kg

- Please refer to the attached drawing for details. (P20)
- Don't guarantee other than shipment by the palette.

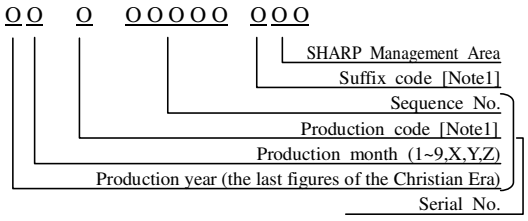
6.2. Label

a) Open Cell label

This label is pasted on the S-PWB. Please refer to the attached drawing for the pasting area. (P19)

ex) LK315D3HA9K

How to express Lot No.



[Note1] Production Code & Suffix Code

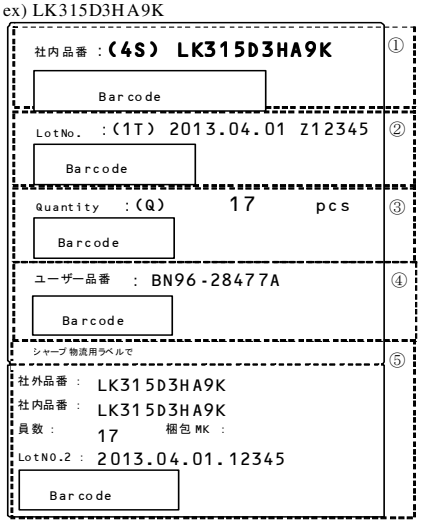
Plant	Model No.	Production Code	Suffix Code
Japan	LK315D3HA9K	L	(non)

b) Packing labels

These labels are stuck on the cell box and palette.

Cell Box Label

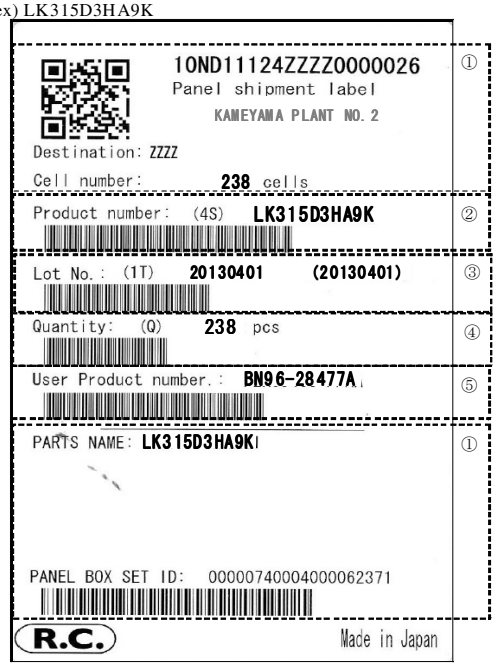
ex) LK315D3HA9K



① Model No.& Suffix Code
② Lot No.
③ Quantity
④ User Code ▲B-3
⑤ SHARP Logistics Management Area

Palette Label

ex) LK315D3HA9K



① SHARP Logostics Management Area
② SHARP Warehousing Code [Note1]
③ Packing Date
④ Open Cell Quantity
⑤ User Code ▲B-3

[Note1] This code may differ from "Model No. & Suffix".

7. Reliability Test Item

No.	Test item (Test sample form)	Condition
1	High temperature storage test (Open Cell)	70°C, 500h
2	Low temperature storage test (Open Cell)	-35°C, 500h
3	High temperature and high humidity operation test (Open Cell)	50°C, 95%RH, 500hr (No condensation)
4	High temperature operation test (Open Cell)	60°C, 500h (With checking Vgl margin variability) (With checking driving part (driver, PCB) temperature by radiation thermometer.)
5	High temperature image sticking test (Open Cell)	60°C with window pattern (5 x 3 cm) 12hr / 72hr / 168hr / 336hr Window pattern is invisible at 60% gray level.
6	Low temperature operation test (Open Cell)	-10°C, 500h (After leaving for 5hr at -10°C, operating at normal condition for 1hr, then operation checking at normal condition.)
7	Turn on after low temperature storage (Open Cell)	After left at low temperature (-10°C) for 24hr or more, operation checking at normal condition.
8	Heat cycle test (Open Cell)	-35°C, 30min <----> 70°C, 30min, 100cycle
9	Press reduction storage test (Open Cell)	15,000ft, -20°C, 10hr
10	ESD test (Open Cell)	Input up to ±15kV 10times from every terminal of CN1 and CN2 with non-operation ▲A
11	Power ON/OFF test (Open Cell)	-10°C and 60°C, ON/OFF time :10sec, 1,000cycle
12	Polarizer moisture absorption test (Open Cell)	0°C, 1hr <---> 30°C, 95%RH, 1hr, 10cycle
13	Flushing test for liquid crystal amount (Open Cell)	140mm or less flushing area by applying pressure at 19.6N/cm^2 after operating at 60°C for 1hr.
14	Vibration test (1 Cell Box with full Open Cells)	X and Y direction: 15min, Z direction: 60min. 5Hz to 50Hz acceleration velocity: 1.0G, Sweeping ratio: 3min
15	Drop test (1 palette with full Open Cells)	Height: 15cm (1 face and 2 sides) Number: 3 times (1 time in each of drop direction)
16	Pad corrosion test (Open Cell in cell box)	50°C, 95%RH, 1,000hr

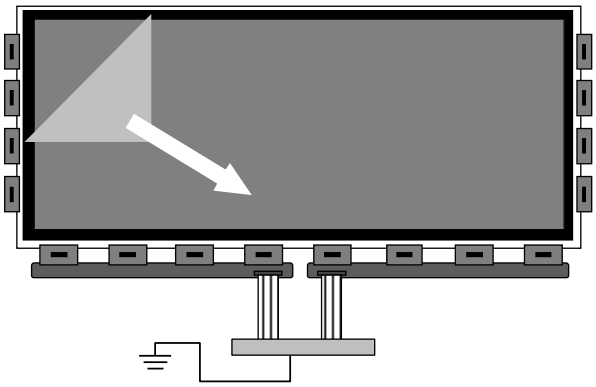
[Result evaluation criteria]

Under the display quality test condition with normal operation state, there shall be no change (except No.5), which may affect practical display function.

8. Precautions

a) Be sure to turn off the power supply when inserting or disconnecting the cable.
b) Be sure to design the cabinet so that the Open Cell can be installed without any extra stress such as warp or twist.
c) Since the polarizer is easily damaged, pay attention not to scratch it.
d) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
e) When the polarizer is soiled, wipe it with absorbent cotton or other soft cloth.
f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
g) The Open Cell has some PWBs, take care to keep them from any stress or pressure when handling or installing the Open Cell, otherwise some of electronic parts on the PWBs may be damaged.
h) When handling the Open Cell and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Open Cell.
i) Applying too much force and stress to PWB and SOF may cause a malfunction electrically and mechanically.
j) The Open Cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufacturers.
k) The chemical compound, which causes the destruction of ozone layer, is not being used.

l) Precautions of peeling off the protection film.



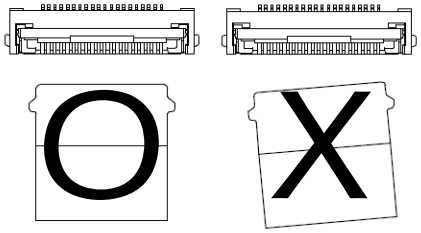
- Be sure to peel off slowly (recommended more than 5sec) and constant speed.
- Peeling direction shows Fig.
- Be sure to ground person with adequate methods such as the anti-static wrist band.
- Be sure to ground all terminals of the S-PWB while peeling of the protection film.
- Ionized air should be blown over during peeling action.
- The protection film must not touch drivers and S-PWBs.
- If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

m) Since the Open Cell consists of TFT and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharges, persons who are handling the Open Cell should be grounded through adequate methods such as the anti-static wrist band. Connector pins should not be touched directly with bare hands.

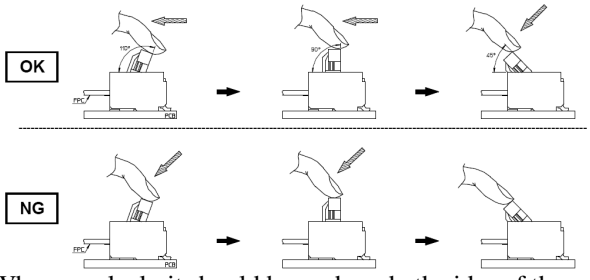
- Reference : Process control standard of sharp

	Item	Management standard value and performance standard
1	Anti-static mat (shelf)	1 to 50 [M ohm]
2	Anti-static mat (floor, desk)	1 to 100 [M ohm]
3	Ionizer	Attenuate from ±1000V to ±100V within 2 sec
4	Anti-static wrist band	0.8 to 10 [M ohm]
5	Anti-static wrist band entry and ground resistance	Below 1000 [ohm]
6	Temperature	22 to 26 [°C]
7	Humidity	60 to 70 [%]

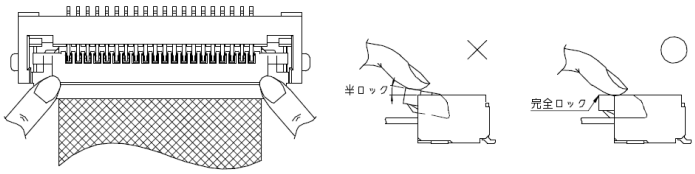
n) Do with the actuator opened completely, and insert it in the interior of the insertion entrance surely horizontally when you insert FPC. (Please put the FPC tab in the ditch of the housing surely with the FPC tab.) Might it become short defective, and it causes the corner to transform the caught terminal into the terminal by the pitch gap when inserting it right and left and diagonally.



o) Please add force in the direction where the actuator is held and do by rotating it pushing in parallel to the S-PWB direction when becoming 90° or less as shown in the figure below until the angle of the actuator becomes 90° or less when you shut the actuator. Please do not add the force to rotary axis of actuator in the direction that the actuator is off.



p) When you lock, it should be push on both sides of the actuator. And it is necessary to confirm that the actuator is surely shut.



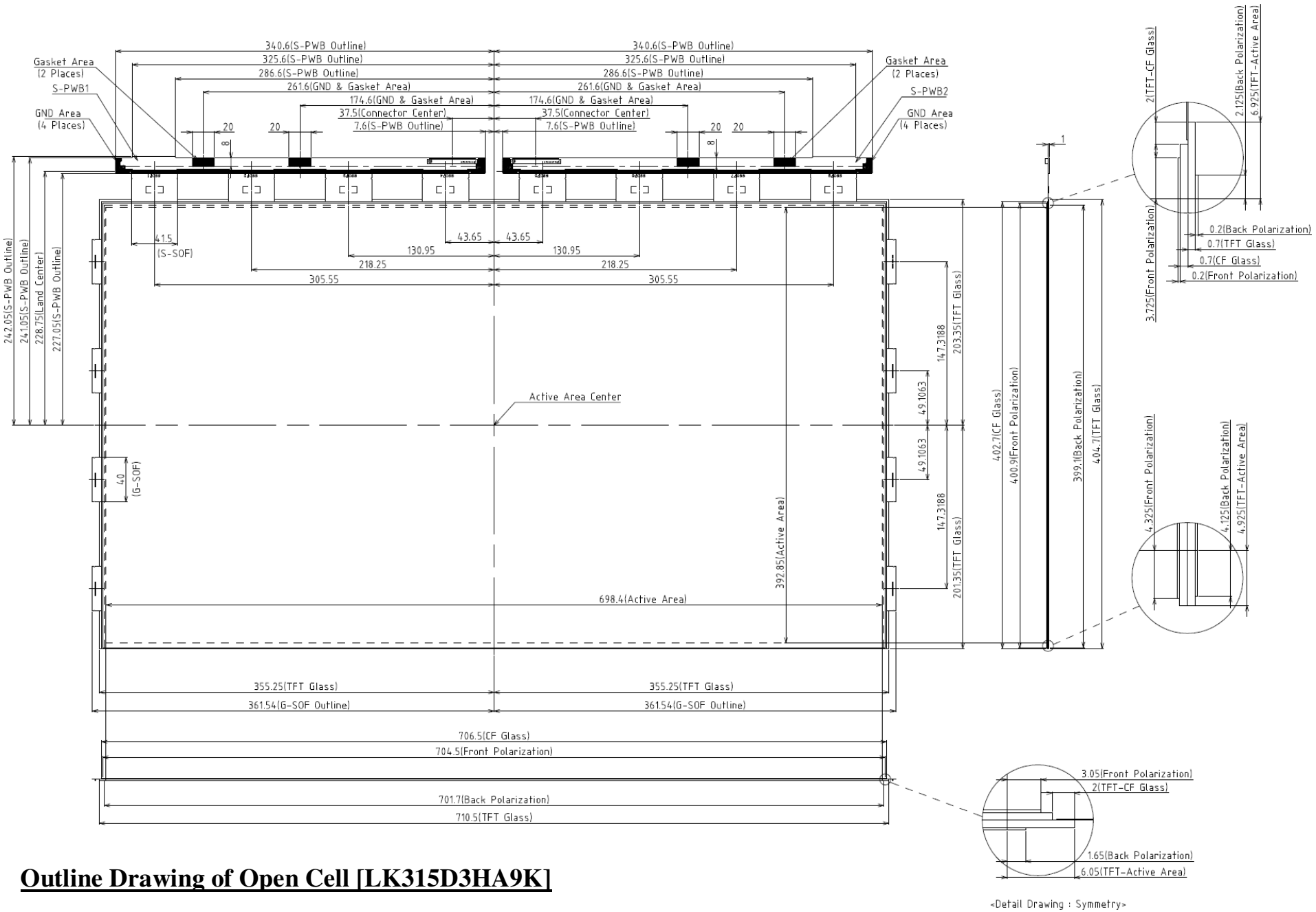
q) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

r) This Open Cell is corresponded to RoHS. "R.C." label on the side of palette shows it.

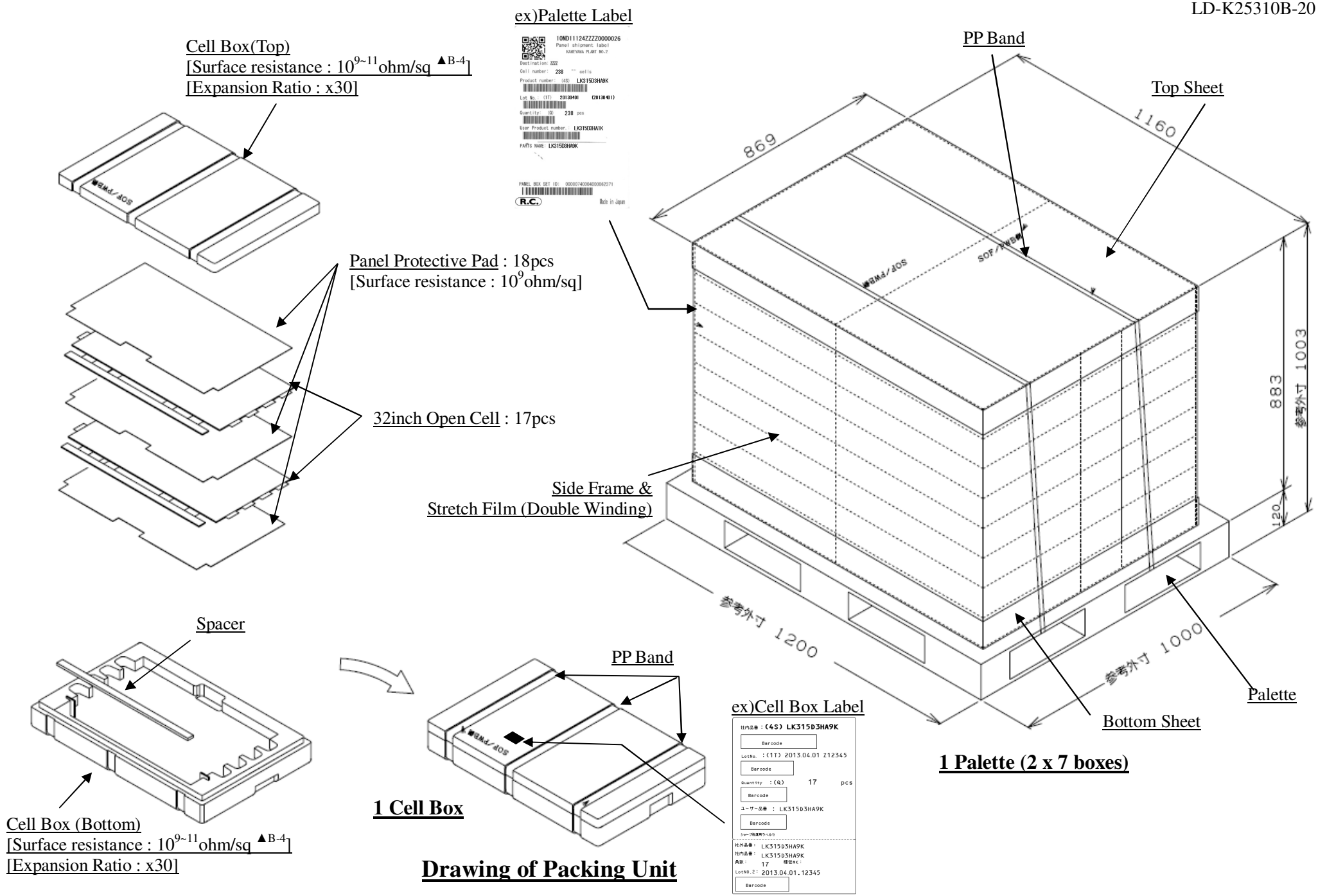
s) When any question or issue occurs, it shall be solved by mutual discussion.

9. Storage Conditions of Open Cell in Cell Box

-	Temperature	0^{o}C to 40^{o}C
-	Humidity	95% RH or less
-	Reference condition	20^{o}C to 35^{o}C, 85% RH or less (summer) 5^{o}C to 15^{o}C, 85% RH or less (winter) The total storage time (40^{o}C, 95% RH) : 240h or less
-	Sunlight	Be sure to shelter a production from the direct sunlight.
-	Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
-	Notes	Be sure to put cartons on palette or base, don't put it on floor, and store them with removing from wall. Please take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
-	Storage life	1 year.



Outline Drawing of Open Cell [LK315D3HA9K]


ex)Palette Label
Cell Box(Top)
[Surface resistance : $10^{9\sim11}$ohm/sq ▲B-4]
[Expansion Ratio : x30]
PP Band
Top Sheet
869
1160
Panel Protective Pad : 18pcs
[Surface resistance : 10^{9}ohm/sq]
32inch Open Cell : 17pcs
Side Frame &
Stretch Film (Double Winding)
883
参考外寸 1003
120
参考外寸 1200
参考外寸 1000
Palette
Bottom Sheet
Spacer
PP Band
ex)Cell Box Label
Cell Box (Bottom)
[Surface resistance : $10^{9\sim11}$ohm/sq ▲B-4]
[Expansion Ratio : x30]
1 Cell Box
1 Palette (2 x 7 boxes)
Drawing of Packing Unit